

40Gbps QSFP+ 40km Transceiver

Product Features:

- 4 channels full-duplex transceiver module
- Up to 11.2Gbps data links per channel
- Maximum link length of 40Km
- 4 CWDM lanes MUX/DEMUX design
- Built-in digital diagnostic functions
- Hot-pluggable QSFP+ form factor
- Single 3.3V power supply
- Operating temperature: 0°C to 70°C
- RoHS 6 compliant(lead free)
- Digital Diagnostic Monitor(DDM)
- Power Consumption < 3.5W



Applications:

- Switch, Router
- 4CH SDR, DDR and QDR
- Client-side 40G Telecom connections

1. General Description

The QSFP-40G-ER4 is a transceiver module designed for 40km optical communication applications. The design is compliant to 40GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically demultiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface

according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

The QSFP-40G-ER4 converts the 4-channel 10Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 10Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	0	70	degC	
Relative Humidity (non-condensation)	RH	0	85	%	
Operating Case Temperature	Topc	0	70	degC	
Operating Range		20	40	km	
Supply Voltage	VCC	-0.5	3.6	V	

4. Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	P _T	-	-	18	dBm	
Average Launch Power, each Lane		3	-	7	dBm	
Optical Modulation Amplitude, each Lane	OMA	3	-	7	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	3.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-4.8	-		dBm	
TDP, each Lane	TDP			2.3	dB	
Extinction Ratio	ER	3.5	-	-	dB	
Relative Intensity Noise	R _{in}	-	-	-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance		-	-	20	dB	
Transmitter Reflectance	R _T			-12	dB	
Transmitter Eye Mask		{0.25,0.4,0.45,0.25,0.28,0.4}				

Definition {X1, X2, X3, Y1, Y2, Y3}						
Average Launch Power OFF Transmitter, each Lane	P_{off}			-30	dBm	
Receiver						
Center Wavelength	λ_c	1260	1310	1360	nm	
Damage Threshold	TH_d	5			dBm	1
Average Power at Receiver Input, each Lane		-13.7		2.3	dBm	
Receiver Reflectance	R_R	-	-	-26	dB	
Receiver Power (OMA), each Lane		-	-	3.5	dBm	
Stressed Receiver Sensitivity in OMA, each Lane		-	-	-12	dBm	
Receiver Sensitivity, each Lane	S_R	-	-	-14	dBm	
Difference in Receive Power between any two Lanes (OMA)				7.5	dB	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane				12.3	GHz	
Signal Loss Assert Threshold	LOSA	-22			dBm	
Signal Loss Dessert Threshold	LOSD			-18	dBm	
LOS Hysteresis	LOSH	0.5		6	dBm	
Conditions of Stress Receiver Sensitivity Test ²						
Vertical Eye Closure Penalty, each Lane			1.6		dB	
Stressed Eye Jitter, each Lane			0.3		UI	

Notes:

- 1.The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
- 2.Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

5. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc1, VccTx, VccRx	3.1		3.47	V	
Supply Current	Icc			1.13	A	
Link turn-on time						
Transmit turn-on time				2000	ms	2
Transmitter (per Lane)						
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	120		1200	mVpp	3
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE P802.3ba, Section 86A.4.1.1			dB	4
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask coordinates {X1, X2 Y1, Y2}		0.11, 0.31 95, 350			UI mV	5
Receiver (per Lane)						
Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	200		400	mVpp	6, 7
		300		600		
		400	550	800		
		600		1200		
AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHz				5	%	
Differential output return loss		Per IEEE P802.3ba, Section 86A.4.2.1			dB	4
Common mode output return loss		Per IEEE P802.3ba, Section 86A.4.2.2			dB	4
Output transition time, 20% to 80%		28			ps	

J2 Jitter output	Jo2			0.42	UI	
J9 Jitter output	Jo9			0.65	UI	
Eye mask coordinates #1 {X1, X2, Y1, Y2}		0.29, 0.5 150, 425			UI mV	5
Power Supply Ripple Tolerance	PSR	50			mVpp	

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. From power-on and end of any fault conditions.
3. After internal AC coupling. Self-biasing 100 differential input.
4. 10 MHz to 11.1 GHz range.
5. Hit ratio = 5×10^{-5} .
6. AC coupled with 100 differential output impedance.
7. Output voltage is settable in 4 discrete steps via I2C. Default is 400 – 800 mV.

6. Transceiver Block Diagram

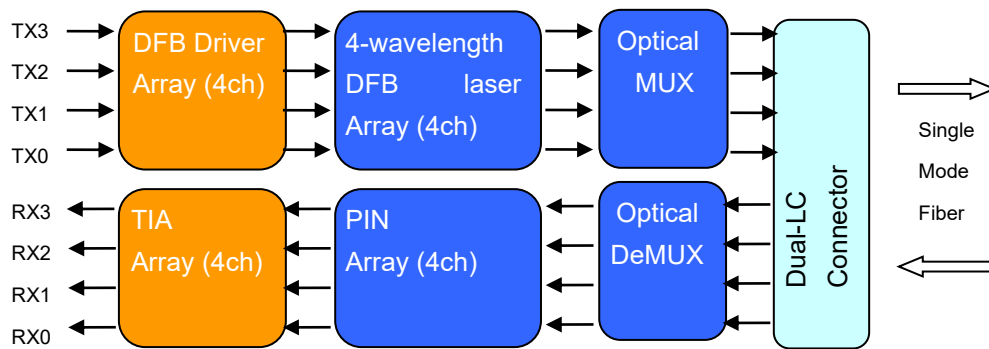


Figure 1: 40Gb/s QSFP LR4 Transceiver Block Diagram

7. Pin Assignment and Pin Description

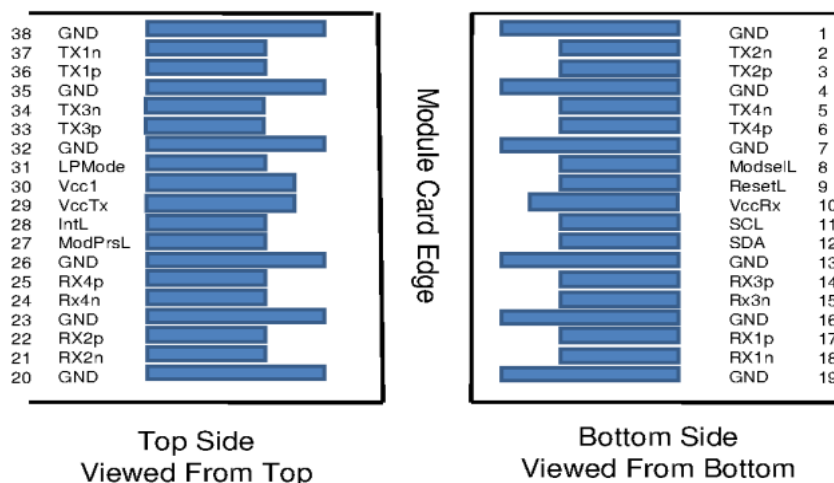


Figure 2 QSPF+ Module Pad Layout

Pin Definitions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1

21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

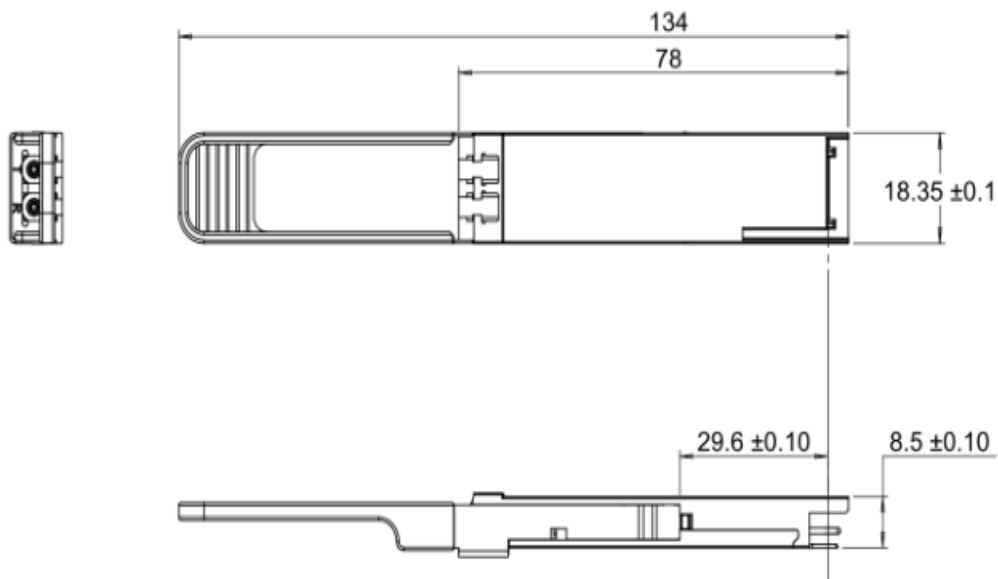
Notes:

1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

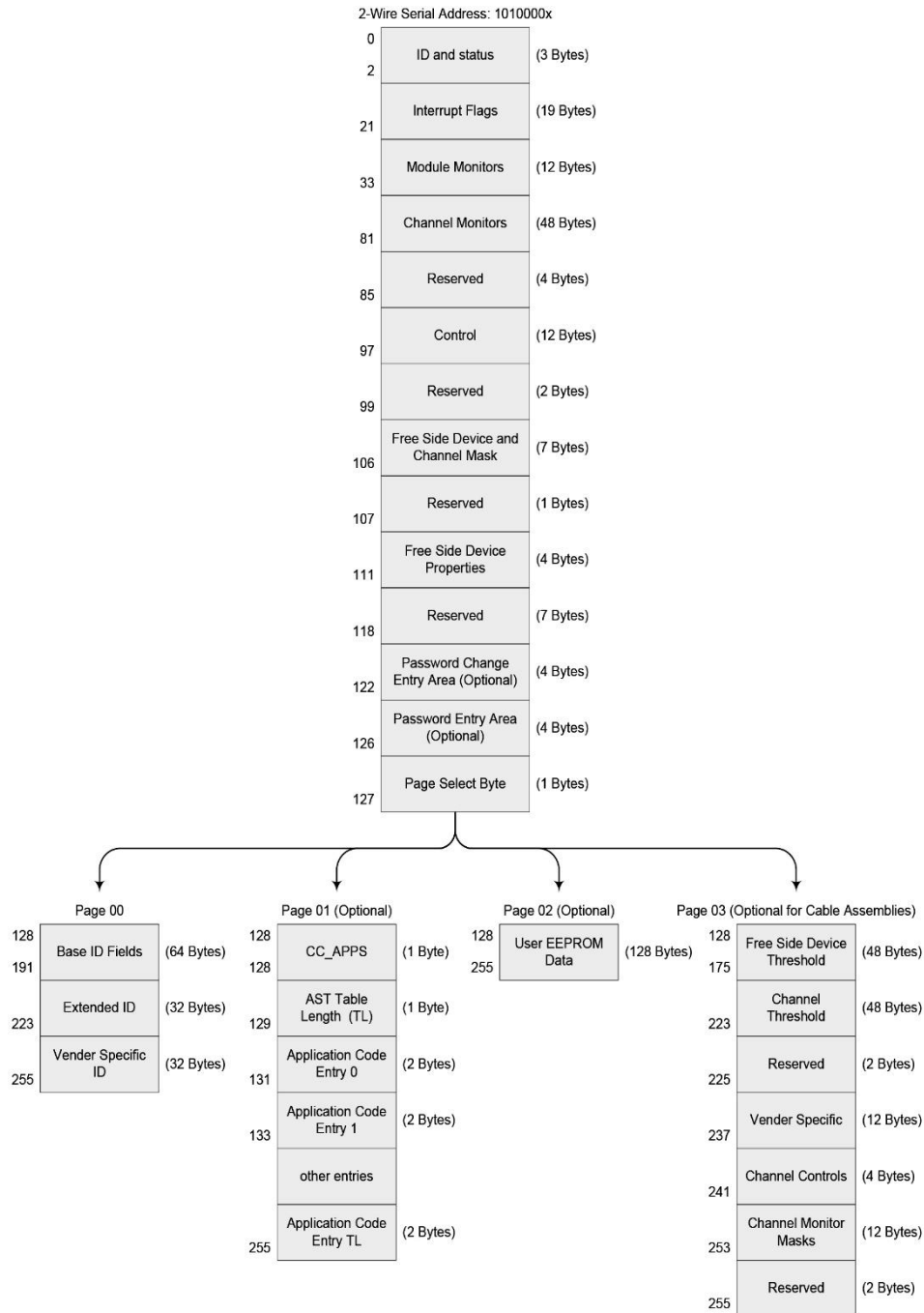
Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

8. Mechanical Design Diagram



9. QSFP+ Memory Map



Ordering Information

Part No.	Data Rate	DDM	Wave	Fiber Type	Dist.	Temp.	Optical Interface
QSFP-40G-ER4	40Gbps	yes	1310nm	SMF	40km	0~70℃	LC

NOTICE:

Connlight reserves the right to make changes to this product in this specification without notice, in order to improve product performance.