100Gbps QSFP28 BIDI 40km Simplex LC Transceiver

Features

- QSFP28 MSA compliant
- 100G Lambda MSA 100G-ER1 Specification compliant

  Interoperable with IEEE 802.3cu
- Supports 53.125Gbaud
- Simplex LC connector
- 4x25G electrical interface (OIF CEI-28G- VSR)
- Single +3.3V power supply operating, Maximum power consumption 4.5W
- Temperature range 0°C to 70°C
- RoHS Compliant

Applications

- Data Center Interconnect
- 100G Ethernet
- Enterprise networking

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	°C
Supply Voltage	$V_{CC}T$, R	-0.5		4	V
Relative Humidity	RH	0		85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_C	0		+70	°C
Supply Voltage	$V_{CCT, R}$	+3.13	3.3	+3.47	V
Supply Current	I_{CC}			1300	mA
Power Dissipation	PD			4.5	W

Electrical Characteristics (TOP = 0 to 70 °C, VCC = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate per Channel		-	25.78125		Gbps	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			35	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		Vcc	V	1
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	150		1200	mV	
Transmit Input Diff Impedance	ZIN	85	100	115		
Data Dependent Input Jitter	DDJ		0.3		UI	
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo	370	600	950	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1
Total Jitter	TJ		0.3		UI	

Note:

1. 20~80%

Optical Characteristics(TOP = 0 to 70 °C, VCC = 3.0 to 3.6 Volts)

Parameter		Symbol	Min	Typ	Max	Unit	Ref.
Transmitter							
Wavelength Assignment	Tx	λ	1304.06	1304.58	1305.1	nm	
	Rx		1308.61	1309.14	1309.66		
Side-mode Suppression Ratio		SMSR	30	-	-	dB	
Average Launch Power		PT	1.5	-	7.1	dBm	
Outer Optical Modulation Amplitude (OMAouter)		P_{OMA}	4.5		7.9	dBm	
Launch Power in OMAouter minus Transmitter and Dispersion Eye Closure (TDECQ)			1			dBm	ER≥4.5dB
Launch Power in OMAouter minus Transmitter and Dispersion Eye Closure (TDECQ)			1			dBm	ER<4.5dB
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ)		TDECQ	-	-	3.9	dB	

Extinction Ratio		ER	6				
Optical Return Loss Tolerance			-	-	20	dB	
Average Launch Power OFF Transmitter,		Poff			-30	dBm	
Relative Intensity Noise		Rin			-136	dB/HZ	1
Optical Return Loss Tolerance			-	-	12	dB	
Receiver							
Wavelength Assignment	Tx	λ	1308.61	1309.14	1309.66	nm	
	Rx		1304.06	1304.58	1305.1		
Total Damage Threshold		THd	-2.4			dBm	1
Average Power at Receiver Input,		R	-16.2		-3.4	dBm	
Receiver Sensitivity	TECQ≤1.4	Rxsens			-14	dBm	1
	1.4≤TECQ≤3.6	SRS			-15.4+TECQ	dBm	
RSSI Accuracy			-2		2	dB	
Receiver Reflectance		Rrx			-26	dB	
LOS De-Assert		LOS_D			-16	dBm	
LOS Assert		LOS_A	-26			dBm	
LOS Hysteresis		LOS_H	0.5			dB	

Note

1. 12dB Reflection

Timing for Soft Control and Status Functions

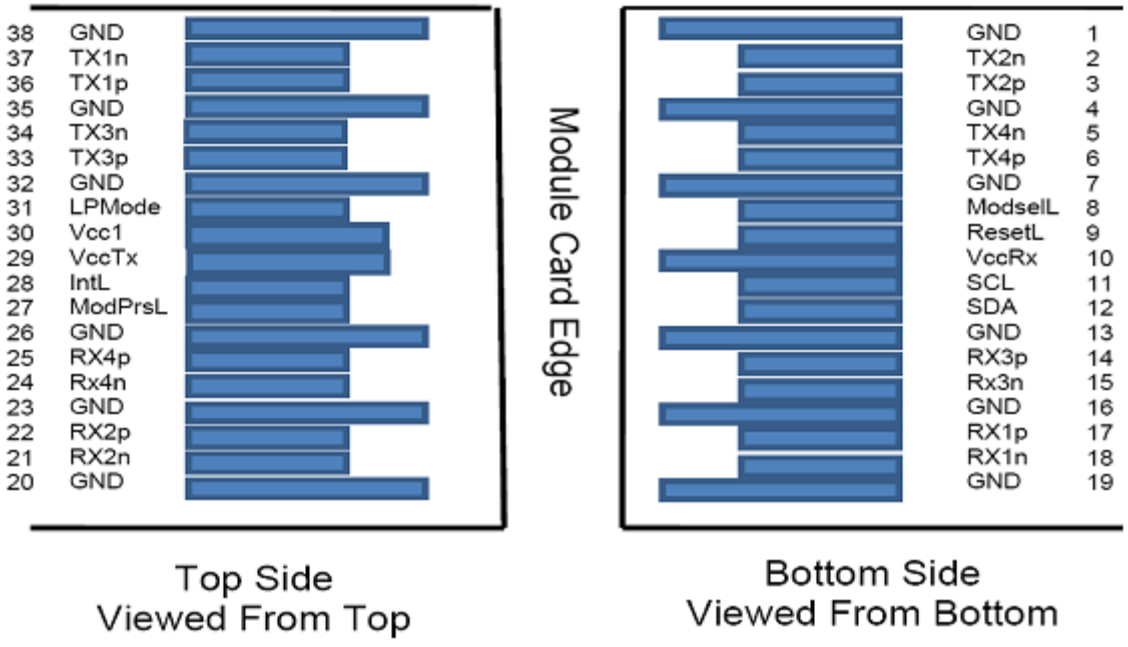
Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read3 operation of associated flag until Vout:IntL =

				Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Pin layout



Pin Definitions

Table 6- Pin Descriptions

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5		NC		3	
6		NC		3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14		NC		3	
15		NC		3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24		NC		3	
25		NC		3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33		NC		3	
34		NC		3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	

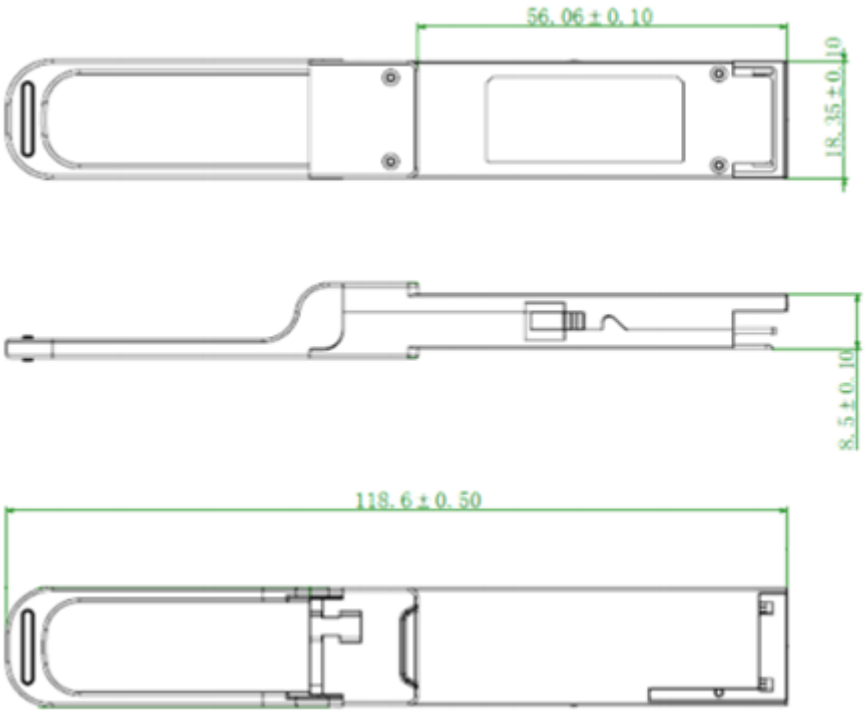
38		GND	Ground	1	1

Note :

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2.Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.

Mechanical Specifications



Ordering Information

Part No.	Data Rate	Laser	Fiber Type	Distance	Optical Interface	Temp
Q28-100G-BX40-U	106.25Gbps	Tx1304/Rx1309	SMF	40km	LC	0~70C
Q28-100G-BX40-D	106.25Gbps	Tx1309/Rx1304	SMF	40km	LC	0~70C

E-mail: info@connlight.com
Web: www.connlight.com